The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.
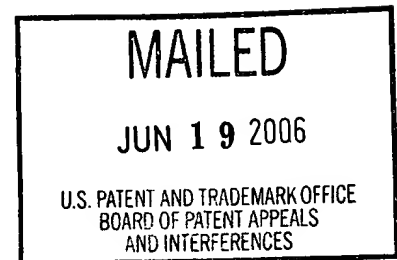
UNITED STATES PATENT AND TRADEMARK OFFICE

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Ex parte BRIAN A. DAY

Appeal No. 2006-1358
Application No. 09/589,930

ON BRIEF

Before JERRY SMITH, LEVY, and BLANKENSHIP, **Administrative Patent Judges**.

JERRY SMITH, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-12, which constitute all the claims pending in this application.

The disclosed invention pertains to a test circuit for inclusion on an integrated circuit. Specifically, the circuit enables real-time testing of a data receiver by identifying a data unit other than a next data unit to be transferred in a data sequence and generating an erroneous data verification parameter that does not verify the data content of the identified data unit. The identified data unit is later transmitted with the erroneous data verification parameter in real time following the transmission of other data units having valid data verification parameters. Such a system allows the user to predefine the occurrence of a real-time error condition that occurs after the successful transmission of multiple data words that included valid data verification parameters.

Representative claim 1 is reproduced as follows:

1. A test circuit for inclusion on an integrated circuit comprising:

a data unit identifier for identifying a data unit other than a next data unit to be transferred in a data unit sequence; and

an erroneous data verification parameter generator for generating an erroneous data verification parameter corresponding to said data unit identified by said data unit identifier, said corresponding erroneous data verification parameter signifying non-verification of data content of said identified data unit.

The examiner relies on the following reference:

Khan   4,561,095   Dec. 24, 1985

The following rejection is on appeal before us:

Claims 1-12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Khan.

Rather than repeat the arguments of appellant or the examiner, we make reference to the brief and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellant's arguments set forth in the brief along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the disclosure of Khan does not fully meet the invention as set forth in the claims on appeal. Accordingly, we reverse.

We consider first the examiner's anticipation rejection of claim 1. Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

The examiner has indicated how the claimed invention is deemed to be fully met by the disclosure of Khan [answer, pages 3-7]. Appellant argues that Khan does not teach identifying a data unit of a data unit sequence where the identified data word is not a next data unit of the data unit sequence [brief, page 6]. Specifically, appellant argues that Khan merely outputs a particular data word stored in random access memory (RAM) along with related stored parity bits to create a check word that allows correction of the outputted data word [brief, page 8]. Appellant contends that such a system only identifies an individual data word stored in RAM for correction -- not a data unit other than a next data unit to be transferred in a data unit

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sequence as claimed [brief, page 8]. Appellant also argues that Khan's RAM does not provide a data unit sequence as performed in data communications circuitry [brief, pages 7 and 8].

The examiner responds that during special error correction circuit test modes in Khan, data words inputted to input lines D_0-D_3 do not constitute a next data unit of the data unit sequence because the identified data unit is not stored in memory, but rather for testing purposes only [answer, page 8]. The examiner also argues that Khan discloses a data unit sequence since (1) the reference teaches inserting a parity code into a sequence of data words inputted to lines D_0-D_3, and (2) the input set of words is inherently a sequence since the words "inherit their ordering from their intended location in memory" [answer, pages 7 and 8].

We will not sustain the examiner's rejection. We agree with appellant that Khan's error correction testing system only identifies an individual data word stored in RAM for correction -- not a data unit other than a next data unit to be transferred in a data unit sequence as claimed. In Khan, error insert means 30 causes a selected bit in the input data word D_0-D_3 to switch to an opposite or erroneous state after encoding the parity word. The error is inserted, however, before the data word is inputted

to and stored in memory array 12 [Khan, col. 6, lines 60-68].
Accordingly, Khan selects and changes a desired bit from an
inputted data word and stores the resulting erroneous data word
in memory to ultimately test the error correction circuitry with
the erroneous word. Contrary to the examiner's assertion, the
identified data unit in Khan is, in fact, written to memory.

On this record, we fail to see how Khan's testing circuit
identifies a data unit <u>other than</u> a next data unit to be
transferred in a data unit sequence as claimed. Khan's system,
at best, identifies only the next data unit to be transferred
when testing the error correction circuitry with the
deliberately-generated errors. Consequently, Khan fails to
disclose every recited limitation of claim 1 either expressly or
inherently and therefore fails to anticipate the claim.
Therefore, we will not sustain the examiner's rejection of claim
1.

Because independent claim 7 contains similar limitations as
claim 1 related to identifying a data unit other than a next data
unit to be transferred in a data unit sequence that are absent in
Khan, we do not sustain the examiner's rejection of claim 7 on
this record for the same reasons discussed above with respect to
claim 1. Since we have not sustained the examiner's rejection of

independent claims 1 and 7, we likewise do not sustain the rejection of dependent claims 2-6 and 8-12.

In summary, we have not sustained the examiner's rejection with respect to any of the claims on appeal. Therefore, the decision of the examiner rejecting claims 1-12 is reversed.

REVERSED

Jerry Smith
JERRY SMITH   )
Administrative Patent Judge   )
)
)
) BOARD OF PATENT
STUART S. LEVY   )
Administrative Patent Judge   )   APPEALS AND
)
) INTERFERENCES
)
HOWARD B. BLANKENSHIP   )
Administrative Patent Judge   )

JS/ce

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